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High capacity and automatic functional extraction tool for industrial VLSI circuit designs

Novakovsky, S. Shyman, S. Hanna, Z.
Intel Corporation

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Abstract
In this paper we present an advanced functional extraction tool for automatic generation of high-level RTL from switch-level circuit netlist representation. The tool is called FEV-Extract and is part of a comprehensive Formal Equivalence Verification (FEV) system developed at Intel to verify modern microprocessor designs. FEV-Extract employs a powerful hierarchical analysis procedure, and advanced and generic algorithms for automatic recognition of logical primitives, to cope with variety of circuit design styles and their complexity. Logic equations are then extracted to generate a behavioral RTL model described in industrial standard HDL languages, to be used in the formal equivalence verification, logic simulation, synthesis and testability flows.

Index Terms
Inspec
Controlled Indexing
CMOS digital integrated circuits VLSI binary decision diagrams circuit CAD design for testability formal verification high level synthesis integrated circuit design logic simulation microprocessor chips theorem proving

Non-controlled Indexing
BDDs DFT FEV-Extract tool Intel **automatic functional extraction** tool automatic generation automatic logical primitives recognition behavioral RTL model circuit design styles formal equivalence verification system generic algorithms hierarchical analysis procedure **high capacity** extraction tool high-level RTL representation industrial VLSI circuit designs industrial standard HDL languages logic simulation logic synthesis microprocessor designs switch-level circuit netlist representation testability flows

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References

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